spin inversion phenomena caused when electrons penetrate the tunnel junction, and the like.

[0060] Now, the examples of the invention will be described.

EXAMPLE 1

[0061] Example 1 relates to the spin tunnel transistor in the first embodiment.

[0062] Initially, the materials for the spin tunnel transistor in the example 1 and the preparing method thereof will be described.

[0063] In the first process, a $CoSi_2$ layer 3 of about 1 nm thickness was formed on a Si substrate 1, and then a base composed of a $Co_{84}Fe_{16}$ layer 5, a Cu layer 7 and a $Co_{84}FeL_6$ layer 9 was formed thereon. A multi-chamber MBE (Molecular Beam Epitaxy) apparatus was used for film formation, and the process was conducted under a pressure of 2×10^{-10} torr.

[0064] First, in the first chamber of the MBE apparatus, a n^+-Si wafer was heated on the side of its (111) substrate surface for about two hours at about 500° C., and subsequently heated for about 0.5 hour at about 700° C. thereby to remove gases adsorbed by the surface.

[0065] Continuously, the wafer was heated to about 840° C. in an atmosphere of diluted Si flux thereby to remove a surface oxide film. At this point of time, the 7×7 structure on the surface of the Si substrate was checked by RHEED (Reflection High Energy Electron Diffraction).

[0066] A non-doped Si layer with a thickness of about 1 μm was formed as a buffer layer on the surface of the Si substrate 1 at about 700° C. After that, stoichiometric amounts of Co and Si were deposited concurrently and the wafer was annealed for about 10 minutes at about 600° C. thereby to form a $CoSi_2$ layer 3 with a thickness of about 1 nm.

[0067] The formation of the $Co_{84}Fe_{16}$ layer 5 (about 2 nm thickness), the Cu layer 7 (about 5 nm thickness) and the $Co_{84}Fe_{16}$ layer 9 (about 2 nm thickness) of the base was carried out in a second chamber by ion beam sputtering. Moreover, the formation of the $Co_{84}Fe_{16}$ layers was conducted during the application of a magnetic field of about 1000 Oe in order to impart uniaxial anisotropy to the two ferromagnetic metal layers 5, 9.

[0068] Subsequently, an Al_2O_3 tunnel barrier layer 11 (about 1.5 nm thickness) was formed using an Al source under an O_2 partial pressure of about 10^{-5} torr in a third chamber.

[0069] Then, a CaF_2 interlayer dielectric film of about 200 nm thickness was formed and the resultant dielectric film was subjected to photolithography and etching thereby to make the tunnel junction area between the base and the emitter 50×50 μm^2, followed by forming a stacked emitter (electrode) composed of an Al layer (about 10 nm thickness) and an Au layer (about 100 nm thickness).

[0070] Volt-ampere characteristics of the spin tunnel transistor were measured to determine the current transmittances and MR ratios, while a magnetic field was applied to the transistor in a plane thereof (in the left and right directions in the sheet of **FIG. 1**).

[0071] Consequently, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were respectively about 5.0×10^{-2} and about 314%. In addition, the current transmittance and MR ratio at an emitter voltage of about 2 V were 5.9×10^{-2} and about 289% respectively.

COMPARATIVE EXAMPLE 1

[0072] For comparison with the example 1, an amorphous $CoSi_2$ layer (about 1 nm thickness) was formed on a Si substrate to prepare a spin tunnel transistor having the same structure as that of the example 1 except for the amorphous layer, followed by conducting the measurements of the current transmittances and MR ratios. In the amorphous $CoSi_2$ layer formation, Co and Si were concurrently deposited as in the case of the example 1, and then the resultant layer was left as an amorphous layer without being annealed. The spin tunnel transistor exhibited a current transmittance of 1×10^{-4} and a MR ratio of about 300% with an emitter voltage of 1.5 V. The MR ratio was comparable to that of the spin tunnel transistor in which a crystal $CoSi_2$ was used, whereas the current transmittance was remarkably reduced.

COMPARATIVE EXAMPLE 2

[0073] Using the same process as that in the example 1, a spin tunnel transistor was formed on a Si substrate through a 1 nm-thick Au layer, which had a $Co_{84}Fe_{16}$ layer (about 2 nm thickness), a Cu layer (about 5 nm thickness) and a $Co_{84}Fe_{16}$ layer (about 2 nm thickness) of the base, an Al_2O_3 barrier layer, and an Al emitter layer.

[0074] In regard to the transistor, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were about 2.8×10^{-3} and about 99% respectively. The transistor exhibited a current transmittance one or more orders of magnitude lower than that the transistor of the example 1 did.

EXAMPLE 2

[0075] Example 2 relates to the spin tunnel transistor in the first embodiment.

[0076] A spin tunnel transistor, which had a base composed of a $Co_{84}Fe_{16}$ layer 5 (about 2 nm thickness), a Cu layer 7 (about 5 nm thickness) and a $Co_{84}Fe_{16}$ layer 9 (about 2 nm thickness) as in the case of the example 1, was formed on a Si substrate 1 through a TiN layer 3 of about 1 nm thickness. The TiN layer 3 was made by ion beam sputtering. The formation of the other layers was conducted in the same process as that in the example 1.

[0077] In regard to the spin tunnel transistor, the current transmittance and MR ratio at an emitter voltage of 1.5 V were about 2.5×10^{-2} and about 280% respectively.

[0078] A similar device including a TiC or FeN layer instead of the TiN layer was prepared. In the case of the transistor with a TiC layer, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were about 2.1×10^{-2} and about 260% respectively. With the device with a FeN layer, when the emitter voltage of the transistor was about 1.5 V, the current transmittance and MR ratio were about 1.3×10^{-2} and about 290% respectively.